

## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

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<b>Title of Invention</b>	SRAM BUS ARCHITECTURE AND INTERCONNECT TO AN FPGA
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Application Number : 10/802577

Confirmation Number: 3499

First Named Applicant: William Plants



Attorney Docket Number:

Art Unit: 2111

Examiner: Gopal C. Ray

Search string:

( 4277844 or 4758745 or 4930097 or 5187392 or 5208491 or 5222066 or 5365485 or 5375089 or 5611042 or 5744979 or 5744980 or 5761140 or 5801547 or 5809281 or 5815003 or 5815004 or 5821776 or 5825200 or 5825201 or 5825202 or 5825662 or 5828230 or 5828538 or 5831448 or 5835998 or 5838167 or 5838584 or 5838954 or 5847441 or 5848005 or 5850151 or 5850152 or 5850564 or 5852608 or 5859542 or 5859543 or 5859544 or 5861761 or 5869981 or 5870586 or 5880492 or 5880512 or 5880597 or 5880598 or 5883526 or 5883850 or 6049487 or 6237124 ).pn

## US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
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	3	4930097	1990-05-29	Ledenbach et al.	A	364	716
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Signature

Examiner Name	Date
Gopal C. Ray	5/16/05